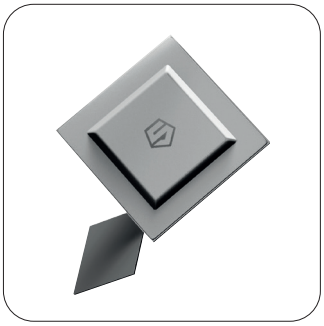
SuperTest - helping to lead the RISC-V revolution at SiFive

California-based SiFive is a semiconductor IP company founded in 2015 by the inventors of the open RISC-V instruction set architecture. Its semiconductor IP ranges from high-performance application processors and vector processors to low-power embedded 64- and 32-bit microcontrollers. SiFive was the first company to design a quad-core RISC-V CPU capable of running fully featured Linux distributions. SiFive generates revenue by licensing its RISC-V processor core IP. The company's HiFive development boards are supported by an IDE that includes a GCC and LLVM compiler toolchain.

SiFive is currently building a new infrastructure to support accelerated ASIC and FPGA design flows, IP delivery, and SoC development. These new developments include state-of-the-art compiler algorithms, novel build system integration, and new Verilog RTL generation techniques. SiFive needed a powerful compiler test and verification tool, not only to verify the functionality of its existing compiler offering, but also to help develop its new IDE infrastructure. The tool SiFive chose was SuperTest.



"Several of the new developers we hired over the last few years already had experience using SuperTest, so we started with a very good understanding of what it was capable of," said Sam Grove, Director, Product Management, SiFive. "It has already helped us to build and verify a high-quality toolchain that our customers can use straight out of the box."

Sam and his team currently use SuperTest for verification and testing of the GCC and LLVM compilers and libraries it supplies with its IDE, as well as for regression and release testing. "SuperTest takes virtually no effort to set up and use," said Richard Fuhler, Director, Compiler Development, SiFive. Over the two years the company has been using it, SuperTest has helped to identify several previously unknown code generation errors in both compiler systems.

Leading the RISC-V revolution

With its origins in the original research that led to the RISC-V architecture, SiFive is the leading provider of RISC-V IP and one of the leading contributors at RISC-V International, the non-profit organization that supports the free and open RISC-V instruction set architecture and extensions. The attractions of RISC-V are two-fold. Firstly, the ISA is license free, removing the cost barrier for adoption by commercial, research or academic users. Secondly, the architecture is modular, extensible and customizable, allowing the addition of unique application-specific instructions and hardware acceleration features at the architecture level, while also leveraging the benefits of industry-wide development of ratified standards for extensions.

For example, SiFive has recently introduced its SiFive Intelligence X280, which extends RISC-V with SiFive Intelligence Extensions that integrate dedicated AI acceleration technology and extended data type support into the RISC-V instruction set architecture. With comprehensive support for TensorFlow Lite, the result is a programmable, scalable, and configurable platform to meet modern AI/ML processing requirements from the edge to the cloud, providing out-of-the-box compatibility with a wide range of popular machine learning models.

Because adding application-specific instructions has implications for the compiler and potentially also the libraries, similar enhanced RISC-V architecture developers may want to take advantage of SuperTest's comprehensive verification capabilities, notably its CGTrainer code generator trainer, which provides a systematic way of testing a modified compiler's back-end. In such situations, SuperTest also provides a way of checking that the basic functionality of the compiler – its correct implementation of the C or C++ language specification – is not broken by the addition of these new instructions.

SiFive

As the pioneers who introduced RISC-V to the world, SiFive is transforming the future of compute by bringing the limitless potential of RISC-V to the highest performance and most data-intensive applications in the world. SiFive's unrivaled compute platforms have enabled leading technology companies around the world to innovate, optimize and deliver the most advanced solutions of tomorrow across every market segment of chip design, including artificial intelligence, machine learning, automotive, data center, mobile, and consumer.

Solid Sands

Solid Sands is the leading provider of compiler and library testing and qualification technology in North-America, Europe and Asia. Our mission is to put quality into C. We do that by improving the quality of C and C++ compilers, libraries and analysis tools, and by enabling their safe and secure use. With the quality level of our test suites, we stay at the forefront of software testing and qualification to help you achieve ISO compliance and functional safety standard requirements. Founded in 2014, Solid Sands is headquartered in Amsterdam, The Netherlands. With partners all over the world we serve both leading innovative companies in the semiconductor, IP and security industries as well as safety-critical companies in automotive, robotics, railway and medical.
Our SuperTest Compiler Test and Validation Suite provides a complete validation environment which enables customers to achieve the software quality level demanded by the ISO language and functional safety standards. Meanwhile, our SuperGuard C Library Safety Qualification Suite is a requirements-based test suite for the C standard library with full traceability between the requirements derived from the ISO C language definition and the individual library tests.

SOLID SANDS

from Amsterdam is the one-stop shop for
C and C++ compiler and library testing,
validation and safety services.

Postbus 7897 | 1008 AB AMSTERDAM | The Netherlands | www.solidsands.nl